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Department of Information Technology (B.Sc. IT)

LESSON NOTES

MICROPROCESSOR AND ALP

Subject Code:
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Unit:
III

SYLLABUS

1	Intel 386 and 486 Microprocessor
2	486DX Architecture
3	Register Organization of 486 Microprocessor
4	Memory Organization
5	Operating Modes of Intel 486
6	Virtual Memory
7	Memory Managment Unit
8	Gates
9	Interrupts and Exceptions
10	Addressing Modes of 80486
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INTRODUCTION:

386 microprocessor is introduced in 1985 and 32 bit microprocessor. It consists 275000 transistors. It is a semi conducted device. It will be controlled by clock signals. Memory Management Unit (MMU) is used to manage the memory for all the executions. It has highly pipelined functional units. It has multiple function in this processor.

- Bus Interface Unit (BIU)
- Code Prefetch Unit
- Instruction Decode Unit
- Execution Unit (EU)
- Segmentation Unit
- Paging Unit

Bus Interface Unit:

Which interacts with data by bus. It will interacting with every parts in CPU. It transfers from input to output, output to input, memory to ALU.

Code Prefetch Unit:

It takes instruction from memory and it stores in instruction queue register.

System Address Register:

- GDTR (Global Descriptor Table Register)
- IDTR (Interrupt Descriptor Table Register)
- LDTR (Local Descriptor Table Register)
- TR (Task State Segment Register)

Addressing Modes in 386 Processor:

Register, Immediate, Direct, Index, Scaled, Scaled Index, Based Index, Based Scaled with Index, Based Scaled indexed with Displacement, Register to Register.

Operating Modes in 386 Processor:

i. Real Mode:

It runs 8086 programs.

ii. Protected Mode:

It has multitasking and protection ability. It runs 80286 and 8086 programs. 80386 is available in three versions.

- 386 SX
- 386 SL
- 386 DX

386 DX:

It has 32 non-multiplexed address lines and 32 data lines.

It can access directly 4GB physical memory and 64 TB capacity of virtual memory.

The data transfer rate is 66MB/Sec.

Intel 386 DX has supporting chips for

387 DX – Math Coprocessor

82395 DX – High performance smart cache

82385 DX – High Performance 32 bit DMA Controller

386 SX:

It has 32 bit internal architecture as 386 DX.

It has only 24 address lines and 16 data lines.

It can address 16MB physical memory and addressing capacity of virtual memory is 64 TB.

386 SL:

It is highly integrated microprocessor.

Eg: Small and portable laptops and notebook computers.

It consumes less power. It contains CPU, memory controller and cache controller.

It has 24 address lines and 16 data lines.

Physical memory capacity is 20MB and virtual memory capacity is 64TB.

INTEL 80486 MICROPROCESSOR

486 microprocessor is an advanced high performance 32 bit CMOS microprocessor was introduced in 1989.

It contains a 32-bit CPU with all features of 386 microprocessor enhancements to improve its speed and computing power, a floating-point coprocessor and 8KB or 16KB code and data cache on a single chip.

It contains a circuitry of 1.2 million transistors.

The math coprocessor is same as 80387 math coprocessor but it is integrated on the chip.

Execution of math instruction is three times faster compared to 386 microprocessor and 387 math coprocessor.

80486 is highly pipelined, so it is enable to fetch several instructions at a time.

While it executes one instruction it decodes the other, get operand for the third instruction and fetches the fourth instruction.

The execution time for the instruction will be minimized. It has two versions.

- i. Intel 486 DX
- ii. Intel 486 SX

Intel 486 DX:

It has three versions.

- 486 DX
- 486 DX2
- 486 DX4

It has 32 bit address lines and data lines. It has 8KB code and data cache. It has a memory management unit (MMU).

It has a floating point math coprocessor on a single chip.

The memory addressing capacity of 486DX.

Physical memory is 4GB and virtual memory capacity is 64TB.

Data transfer rate is 106MB/Sec at 33MHZ, 320MB/Sec at 100MHZ.

Intel 486SX:

The memory address capacity of 486 SX is 4GB physical and 64TB virtual.

486 DX ARCHITECTURE

It has 9 functional units.

- Bus Interface Unit (BIU)
- Code Prefetch Unit
- Instruction Decode Unit
- Execution Unit (EU)
- Segmentation Unit
- Paging Unit
- Control and Protection Test Unit
- Floating Point Math Co-Processor Unit (FPU)
- Cache Unit

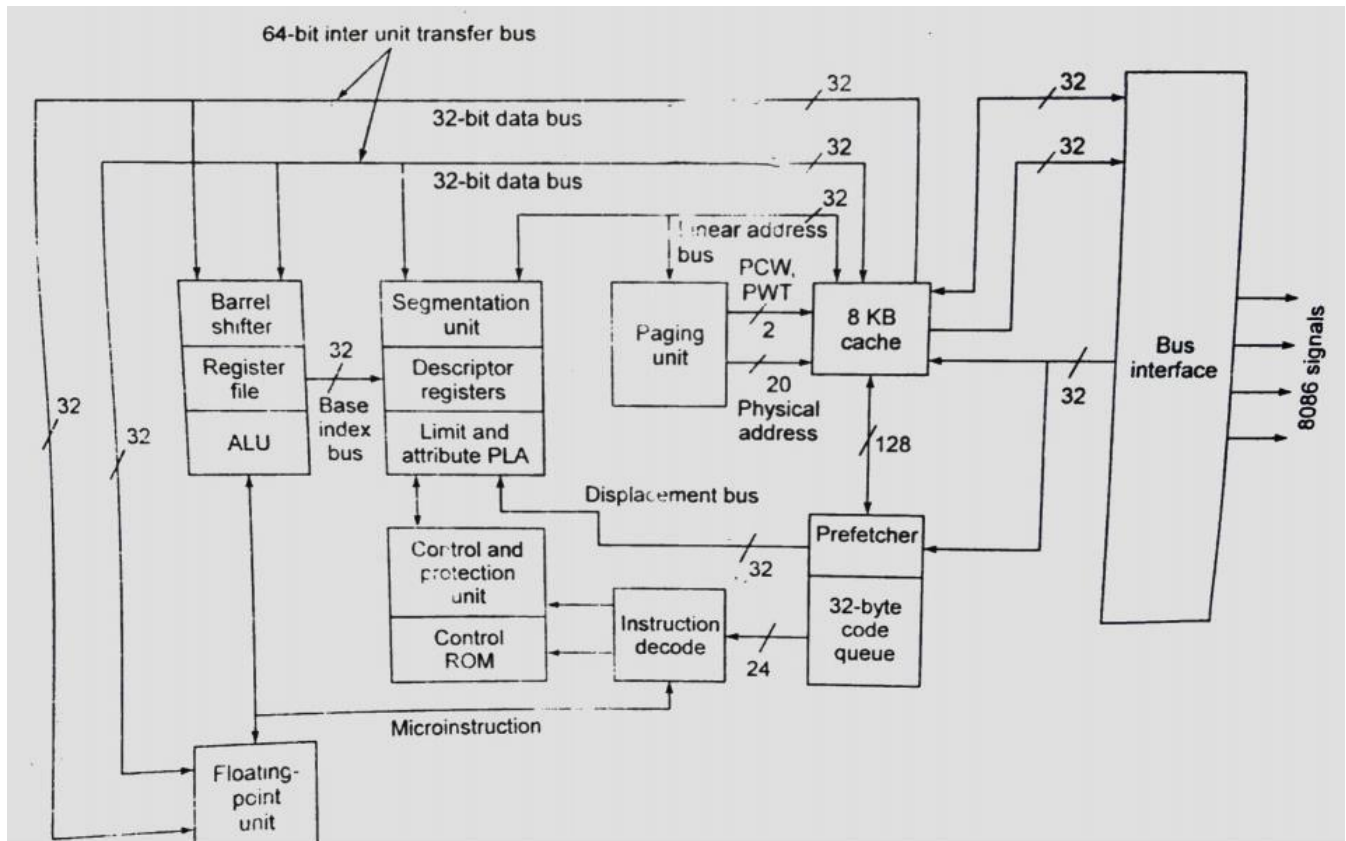
It is highly pipelined.

Execution Unit:

It has barrel shifters, register file and ALU. Barrel shifters are special type of shift register can perform multiple number of shifts in single operation.

Segmentation Unit:

It contains descriptor registers.



Paging Unit:

It contains paging mechanism, translation look aside buffer etc.

Intel 486 has a cache of most recently accessed pages. This cache is called as translation look aside buffer.

Intel 486 has control ROM with control and protection test unit.

Bus Interface Unit:

It contains address drivers, write buffers, data bus transceiver, bus control request sequencer, cache controller, burst bus control.

Bus interface unit interfaces with memory and IO devices to 486 microprocessor.

Code Prefetch Unit:

It fetches instruction and keeps them in a 32 byte code queue.

Instruction Decoding Unit:

It receives codes from prefetch unit and decodes them and the execution unit executes the instructions.

Floating Point Math Coprocessor:

It executes trigonometric, logarithmic, exponential and arithmetic instruction.

It operates on 32, 64 and 80 bit floating point, 32 and 64 bit integers and 18 digit BCD operands.

Memory management unit consists of segmentation unit and paging unit.

Segmentation unit translates logical address into linear address.

Linear Address = Base Address of segment + Offset

Paging unit translates linear address into physical address.

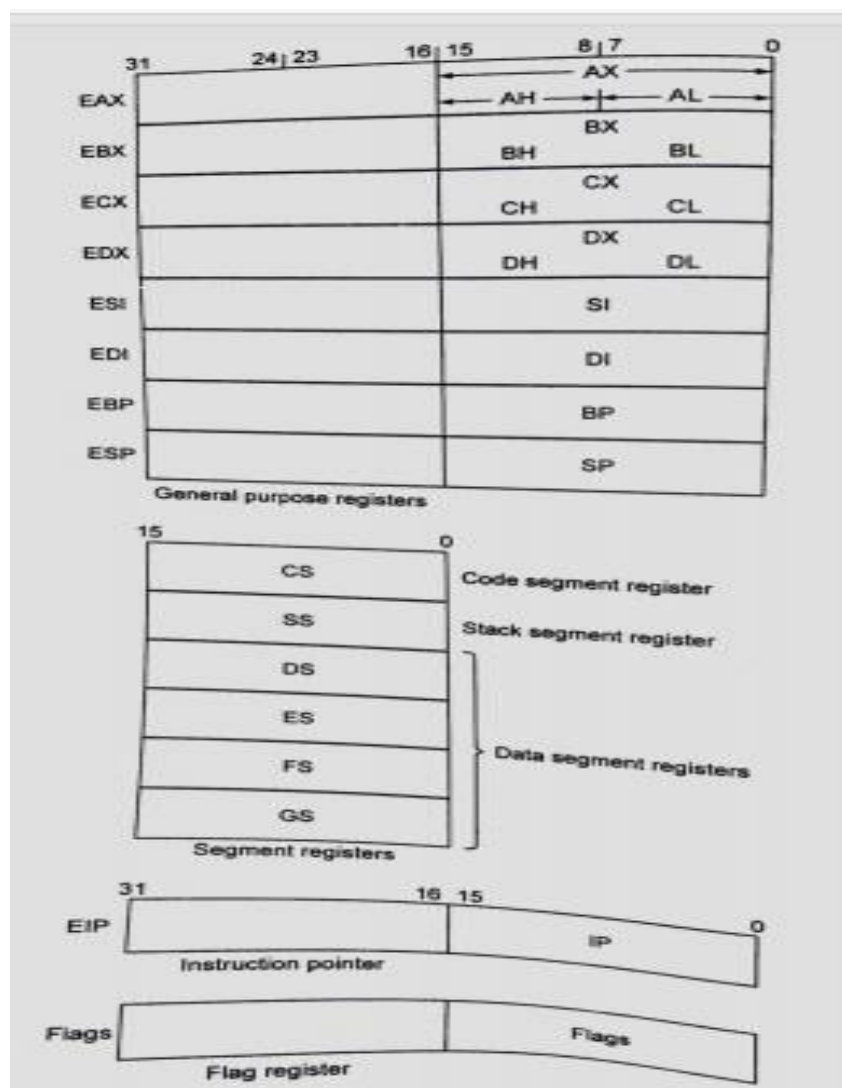
Cache Memory:

Cache is very fast memory unit. It is static RAM. It contains instruction codes and data which are currently being used.

Control and Protection Test Unit:

486 hardware is designed to provide protection mechanism to isolate operating system from user task and each other.

REGISTER ORGANIZATION OF 486 MICROPROCESSOR



It has 8 general purpose register namely,

EAX, EBX, ECX EDX

ESI, EDI, EBP, ESP

E denotes extended memory. It is 32 bit. Low order 16-bit of each general purpose register can be accessed separately.

These registers are called as AX, BX, CX, DX, SI, DI, SP and BP

For 8-bit operation, the registers can be individually accessed. They are AH, BH, CH, DH, AL, BL, CL and DL

It has six segment register. They are CS, ES, DS, SS, FS and GS. It has 16-bits.

Two additional data segment register FS and GS are available in Intel 486.

Totally four data segments are available.

Data segment registers can access four different data areas in the memory and allows the program to access four different data structures.

EIP is a 32 bit register, which holds the effective address of the next instruction which is to be executed.

The offset address in IP is related to the starting address of code segment in CS register.

Low order 16 bit of EIP is used for 16 bit operation and is called IP.

1. Flags of 486 Microprocessor:

E-Flags are 32 bit flag registers. Low order 16 bit can be used for the execution of 16 bit operation and it is called as E-Flag.

E-Flags contain 14 flags. It is divided in two ways. There are,

Conditional Flag (CF, PF, AF, ZF, SF, OF)

Control and System Flag (DF, IF,TF)

Carry Flag:

The carry flag carries the most significant bit of carry over resulted in addition or the borrow resulted during the subtraction.

If the carry bit is available carry flag will be set to 1 else set to 0.

Parity Flag:

It is set to 1 if lower order 8 bit result after execution contains even number of 1 else it will be 0.

Auxiliary Flag:

It is set to 1 if carry out of bit 3 resulting from an addition or if a borrow is needed from bit 4 into bit 3 for subtraction, otherwise set to 0.

Zero Flag:

It is set to 1 if the result of arithmetic or logic expression is zero then the flag is set to 0 otherwise 0.

Sign Flag:

It is set to 1, if the most significant bit of arithmetic operation is 1 then the flag is set to 1. Otherwise the flag is 0.

Overflow Flag:

It is set to 1, if the operation has signed overflow carry or borrow. These are conditional flag.

Control and System Flag:

Directional Flag:

It shows the directions of string operation. If DF is set to 1, ESI and EDI will be decremented to access string from lower memory to higher memory.

Interrupt Flag:

The interrupt can be enabled or disabled using IF. If IF = 1 interrupt INTR is enabled if IF=0 interrupt will be disabled.

Trap Flag/Trace Flag:

Trap or Trace flag is used for debugging the instruction using single step control. If TF=1, the processor will be in single step mode.

Virtual 8086 Mode Flag:

VM is set to 1 while 486 is in the protected mode, the microprocessor will switch over to virtual 8086 operation.

Alignment Check:

It will be set to 1, if the debug fault is ignored.

Nested Task (NT):

In protected mode, the execution of current task is nested within another task NT will be 1.

Input/output Privilege (IOPL):

It has 2 bit flags. This is a flag for protected mode. It shows the maximum privilege level allowed for input and output instruction execution.

2. System Descriptor Cache Register:

CS, SS – Code Segment

GS,DS,ES,FS – Data Segment

It is associated with each segment register. When segment register is loaded the information about the segment is read from the descriptor table and loaded to segment descriptor cache register.

The information consists of 32 bit base address and 32 bit segment limit.

3. System Level Register:

It is used to control the operations of on chip cache, floating point unit (FPU), segmentation and paging mechanism.

Intel 486 has three control registers and four address registers.

i. Control Register:

There are 3 registers available in Intel 486. They are CR0, CR2 and CR3.

ii. System Address Register:

There are 4 address registers. They are,

GDTR (Global Descriptor Table Register)

LDTR (Local Descriptor Table Register)

IDTR (Interrupt Descriptor Table Register)

TR (Task State Segment Register)

GDTR contains 32 bit base address and 16 bit limit value for size of the table.

LDTR contains 16 bit segment selector.

IDTR contains 32 bit base address for IDT and 16 bit value for size of the table.

TR: In multi user or multi-tasking system information about each task is available in TSS. (Task Status Segment)

TSS:

Memory segment which contains the task's state is called TSS.

4. Floating Point Register (FPU):

It has separately 8 data register. It has a tag word. It has a control register, status register, instruction pointer and data pointer.

5. Debugging Registers:

There are 6 debug register is available in Intel 486, namely DR0 – DR3. It holds 4 break points.

DR4 and DR5 for future use.

DR6 – Debug the status register

DR7 – Set the break points.

6. Test Registers:

In Intel 486, 5 test registers are available. They are TR3 – TR7

TR3, TR4, TR5 –control the test of on-chip cache.

TR6 and TR7 – Controls the translation look aside buffer.

MEMORY ORGANIZATION OF INTEL 486

Intel 486 has memory segments. It can handle a byte, word and double word. The memory in real mode is segmented into 64MB of fixed size.

In protected mode the segment size may vary from 1 byte to 4GB. Segmentation is useful for an application programmer as it can organize memory in logical modules.

Paging is useful for a system programmer to manage physical memory of a system.

The failure of software occurs due to the growth of stack instruction code or data of a program. Segmentation prevents this failure as stack segment is separated from code and data segment.

Logical Address: Address in the coding or program.

Linear Address: Base address of segment + Offset address within the segment

Physical Address: Hardware memory RAM/ROM

Since offset address is 32 bit, the size of the segment varies up to $2^{32} = 4\text{GB}$.

In Protected Mode:

The selector as out of 16 bit out of 14 bit are used to address a descriptor in a descriptor table remaining two low order bits (0,1), remaining of the selector indicates the privilege level for the protected mode.

The description table consists of 32 bit base address 20 bit limit of the segment and 12 bit attributes for memory segment.

Out of 14 bits, 13 bits are used as index to the descriptor table LDT and GDT.



The logical address or virtual address up to 64TB. As Intel 486 has 32 address lines. The maximum direct addressing capability is 4GB physical memory RAM and ROM.

In real mode the content of segment register will not given the address directly it add as an access the index to the local descriptor to table LDT or GDT.

Flag Memory Model:

A memory model which eliminates the segmentations and uses the entire memory space in a single block is called flat memory model.

In Intel 486 this flat memory model can be achieved by providing the same base address for all the segments also the segment limit of 4GB is kept for all segment type memory model is called Simple Flat model.

OPERATING MODES OF INTEL 486

The Intel 486 has two operating modes, which are known as, **Real Mode, Protected Mode.**

Real Mode:

The memory addressing capacity is 1MB. Segment register gives the direct addressing with 16 MSB. The direct address will be shifted left by 4 bits and with the result the offset address is added to get the linear address.

Paging is not allowed in real mode.

Real mode is used to set the 486 processor to run in protected mode.

When the processor is switched on or the processor is reset it will be initialized in real mode then the processor will be switched on the protected mode.

The system tables and registers are initialized with appropriate values in the real mode.

Protected Mode:

In protected mode, Intel 486 provides memory management and protection facilities.

32 bit address lines are used to address a memory location.

Memory segment size is variable. It varies from 1 byte to 4GB.

Selector will not give the MSB's of memory address directly. But it gives an index into a descriptor table consists of the base address of the segment, upper limit of segment and other attributes.

The paging unit converts the linear address into physical address.

Along with the segmentation facility, the paging facility is also available in protected mode of Intel 486.

The page oriented system is known as **Page Fault Model or Demand Paged Virtual Memory Scheme.**

The UNIX operating system supports demand paged virtual memory scheme.

Virtual Memory:

In Intel 486 processors 16 bit selector and 32 bit offset is used for memory addressing. Out of 16 bits, 14 bits are used for addressing and other 2 bits are used for privilege level.

The maximum size of segment is 4GB, totally 64TB can be addressed.

Thus 64TB memory space is virtual memory. Using 32 bit address lines 486 microprocessor can address only 4GB of physical memory.

The 64TB memory does not actually exist and is called as virtual memory. If a programmer needs more memory capacity than actual memory while writing a program then the virtual memory technique is used.

The program is stored in a hard disk. The part of the program required for current execution will be loaded into the main memory and the previously executed part of the program will be sent to the secondary memory. The movement of parts of the program from main memory to secondary memory and vice-versa is known as **Swapping**.

ADDRESSING MODES OF INTEL 486

The Intel 486 has 11 addressing modes. Among these 11 addressing modes, 2 addressing modes are register or immediate operand. The other 9 addressing modes will specify the memory operands.

1. Register Addressing Mode:

The operand is one of the 8, 16 or 32 bit general purpose register.

2. Immediate Addressing Mode:

In immediate addressing mode operand is included in the instruction itself.

Effective Address or Offset:

There are 4 addressing elements used to compute the offset or effective address of the operand.

- i. Displacement
- ii. Base
- iii. Index
- iv. Scale

i. Displacement:

Displacement is a 8 bit or 32 bit immediate value given by the user.

ii. Base:

The content of any general purpose register.

iii. Index:

Index is also the content of general purpose register except ESP (Extra Segment Pointer) used as index to point the operand.

iv. Scale or Scaling:

It is a factor to multiply the content of index register. It may be 1, 2, 4 or 8 bit even number.

Effective Address (or) Offset = [Base Register] + [Index Register X Scaling] + Displacement

3. Direct Addressing Mode:

The operands offset is part of the instruction itself. The operands offset will be specified within the instruction as 8, 16 or 32 bit displacement.

4. Register Indirect Addressing Mode:

The base register has the offset of the operand.

5. Based Addressing Mode:

The offset of an operand is computed by adding the content of base register and with displacement.

6. Indexed Addressing Mode:

The operands offset is computed by adding the content of index register and with displacement.

7. Based Index Addressing Mode:

The operands offset is computed by adding the content of base register with index register.

8. Scaled Index Addressing Mode:

To get the operands offset the content of index register multiplied with scaling factor and to the result by adding a displacement.

9. Based Scaled Index Addressing Mode:

The content of index register will be multiplied by the scaling factor and to obtain the result. The content of base register will be added to get the operands offset address.

10. Based Indexed Addressing with Displacement:

Content of base register and content of index register and displacement will be added which gives the operands offset address.

11. Based Scaled Index Addressing with Displacement:

The content of index register will be multiplied by the scaling factor and to the result. The content of base register and displacement will be added which provides the operands offset address.

MEMORY MANAGEMENT UNIT (MMU)

The Intel 486 memory management unit is built in the chip itself. It has 2 functional units. They are segmentation unit and paging unit.

In a multiuser or multitasking environment each task or user should be provided with independent memory areas. So that they will be no interface with each other and with the operating system.

With limited memory space, it is not possible to provide individual memory space for the task separately.

Memory management is needed to allocate memory. Operating system can perform some tasks of memory management, but it cannot provide completely.

MMU is built in chip itself for complete memory management.

Segmentation unit provides 4 levels of protection for isolating and protecting task and the operating system from each other.

Memory Functions of Memory Management Unit:

MMU converts the logical address to corresponding linear address.

The linear address will be converted to physical address.

The functioning can be done by 2 techniques.

- i. Segmentation
- ii. Paging

The segmentation technique can be used to give each program several independent and protected memory areas in a multiuser/multitasking system.

Paging Technique:

It is used together with segmentation technique to divide a segment into smaller memory areas to achieve the faster swapping. If only paging technique is available, it divides the memory space only in smaller sections.

MMU checks if the desire memory segment is in the memory. If the memory space is available in computer, the corresponding physical address and load the program.

If it is not available, it interrupts the CPU. Then operating system loads the desire memory segment from hard disk to main memory to make space in main memory. MMU moves the least used segment back to the hard disk. The movement of segments from hard disk to the main memory and vice-versa is called Swapping.

MMU checks if the desire segment is present in the memory or not.

If the desired segment is present in the memory is called Hit, else it is a Miss.

Advantages of Combined Scheme (Segmentation & Paging):

The desired pages are swapped in and out of the physical memory. The program will be loaded easier. The swapping is a factor.

Disadvantages of Combined Scheme:

The time needed is too large.

The memory capacity require for all the tables is very large.

GATES

User task can access the required software in memory segment which is placed in memory segment which is placed in a restricted way under the control. Operating system can be accessed through gate. Gate is a special type of descriptor. There are 4 types of Gates.

- i. Call Gate
- ii. Trap Gate
- iii. Interrupt Gate
- iv. Task Gate

All gates in a system are specified by the operating system.

Interrupt Gate:

Gate descriptor for interrupt or exception subroutine resides in IDT (Interrupt Descriptor Table). During the process of initialization, the base address and limit for IDT are loaded into IDTR (Interrupt Descriptor Table Register). IDT contains gate descriptor for interrupt, trap and task. If the request for the desired segment is valid then the selector from gate descriptor is loaded into code segment register. Selector loaded in the CS register is used to access the descriptor for desired segment which has interrupt or trap subroutine. Descriptor gives the base address and its limits for the desired segment.

Call Gate:

The call gate descriptor resides in GDT & LDT. When a call occurs the call gate descriptor is fetched from GDT or LDT. This descriptor has a selector, 32 bit offset and privilege level.

The privilege level will be checked if the desired segment is available then the selector from call gate descriptor is loaded into CS register.

Selector is used to find the base address and limit in LDT or GDT.

INTERRUPT & EXECUTION

Interrupts & executions cause forced transfer of program execution to a subroutine or a task.

The interruption of normal program execution accessed by external events as request from peripheral device which is known as hardware interrupt.

The normal program execution can be interrupted by inserting special instruction in program is known as Software Interrupt. Software instructions are caused by INT n, INTO & BOUND instructions. The microprocessor treats software interrupts as exceptions. In 486 microprocessor NMI & INTR are the two interrupt lines.

NMI is a non-maskable interrupt whereas INTR is a maskable interrupt.

Different types of interrupts or exception have been given an identification number. This number is called Interrupt Type or Interrupt Vector. There are 256 types of interrupts/exceptions in a 486 microprocessor based system.

When an interrupt occurs through INTR line, in response of interrupt acknowledge signal, the interrupt controller sends an 8 bit vector which identifies the interrupting I/O device. This 8 bit vector is a pointer to IDT table to find the gate descriptor.

The ways to supply 8 bit interrupt vector for different types of interrupts and exceptions are as follows:

- i. Exceptions provide the interrupt vector internally.

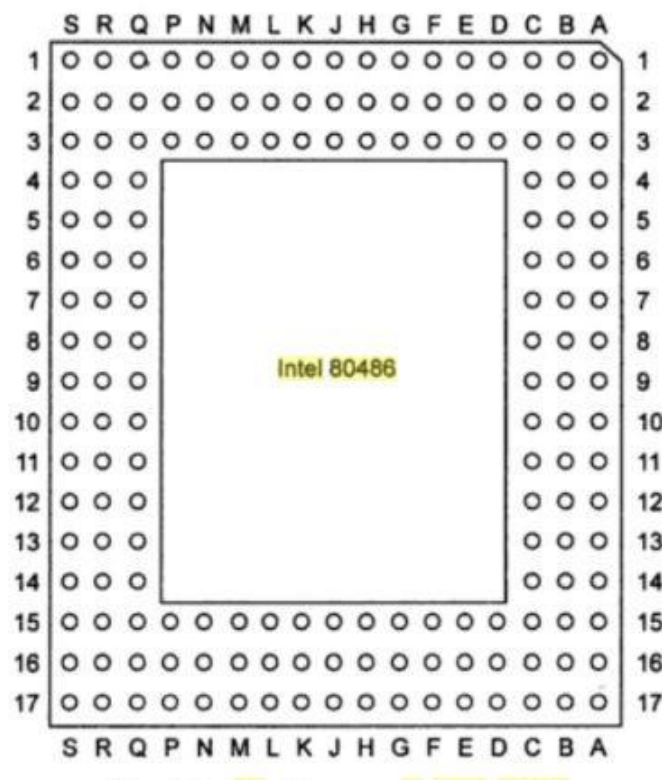
- ii. Software interrupt instruction INTn contains or implies the 8bit vector.
- iii. The maskable hardware interrupt supplies 8 bit vector through interrupt controller in responses to interrupt acknowledgement signal received from the CPU.
- iv. The interrupt vector 2 has been assigned to non-maskable interrupt NMI.

Interrupt & Exception Vectors:

Interrupt Type	Description
0	Divide Error
1	Debug Exception
2	NMI Interrupt
3	Breakpoint
..	...
32 - 255	Available to programmer

PIN CONFIGURATION AND SIGNALS OF 80486

The below mentioned diagram is the Pin diagram of Intel 80486. It is contained in a 168-pin grid array package.

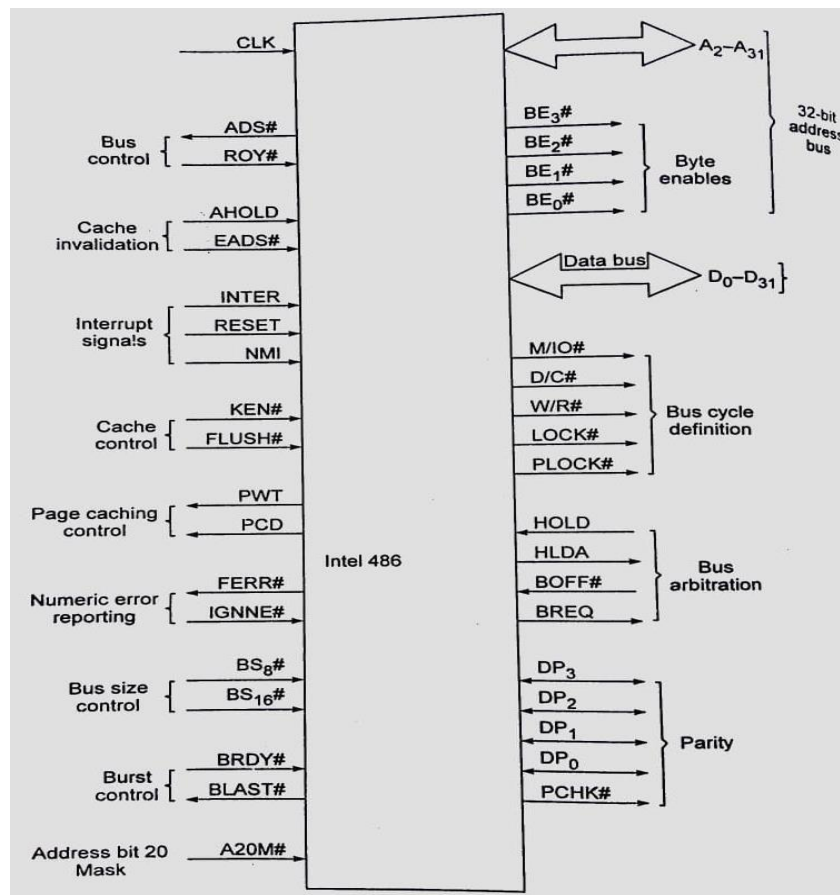


A2 – A3 (output) & A4 – A31 (Input/Output):

A2 – A31 are address lines. They specify memory or I/O address together with byte enable signals.

BE₀ # – BE₃# Output:

These are byte enable signals. They are active LOW signals. They indicate which data bytes of the data bus take part during read & write.



D0 – D31: It is the output data lines.

DP0 – DP3: It send data parity signal for each byte in data lines.

M/IO:

Memory or input/output device access lines.

When this signal is high, CPU access data from memory.

When this signal is low, CPU access data from input/output device.

D/C:

It is an output line.

It controls the data and it is the data control line.

When it is high, it controls data transfer.

When it is low it controls signal transfer.

W/R:

It is output line.

It controls write and read operation.

When the signal is high it performs write operation

When the signal is low it performs read operation.

Lock:

It is output line.

It indicates that the current bus cycle is lock.

It allows address hold but it will not allow bus hold.

Plock (or) Pseudo lock:

It indicates that the current bus transaction needs more than one bus cycle for completion.

ADS:

It is an output signal.

Address status output.

It indicates valid address on the bus.

RDY:

It is an input signal.

Non burst ready signal.

It indicates external device is ready for read or write operation.

ADS and RDY are the bus control signals.

BRDY:

It is an input signal.

Burst ready input.

BLAST:

It is an output signal.

Burst ready last signal.

BRDY and BLAST are the control burst mode memory read or write operation.

RESET:

It is an input signal.

RESET the microprocessor.

INTR:

Input signal.

It is an interrupt line caused by an external device.

NMI:

It is an input line.

It shows the non-maskable external interrupt line.

BREQ:

It is an output line.

It sends internal cycle pending signal.

HOLD:

It is an input line.

Another master device requires the control of the bus.

It sends hold signal to the microprocessor.

HLDA:

It is an output signal.

It is a hold acknowledge.

It issued by the microprocessor after receiving hold signal.

AHOLD:

It is an input line.

Address hold request which allows another master to access the address bus to perform cache invalidation.

EADS:

It is an input line.

Used to cache invalidation for a cycle.

It indicates valid address is placed in the address bus.

KEN:

It is an input line.

It sends the cache enable signal.

It determines whether the current cycle is cacheable or not.

Flush:

It is an input signal.

Cache flush input, it clears the entire internal cache.

PWT:

It is an output signal.

Page write through signal.

It controls the write operation of external cache memory.

PCD:

It is an input line.

Page cache disable signal.

It controls the onchip cache memory when PCD is 0 onchip cache will be enable.

PCD is 1 onchip cache will be disable.

FERR:

It is an output line.

Floating point error signal line.

It is active when floating point error occurs.

IGNNE:

It is an input line.

Ignore numeric error signal.

It ignore the numeric error.

BS16:

It is input line.

Bus size 16 signal, indicates 16 bit data transfer.

BS8:

It is input line.

Bus size 8 signal, it indicates 8 bit data transfer.

A20M:

It is input line.

Address bit 20 maskable.

It masks 20 bit physical address.

TCK:

It is input line.

Test clock, it provides clock function.

BOFF:

It is input line.

It is back off input.

It floats its buses in next clock cycle.

BE1, BE2, BE3 and BE0:

It is output line.

It sends the signal of byte enable.

Table 7.2 Logic for M/IO#, D/C# and W/R#

<i>M/IO#</i>	<i>D/C#</i>	<i>W/R#</i>	<i>Operation</i>
0	0	0	Interrupt acknowledge
0	0	1	Halt/Special cycle
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Code
1	0	1	Reserved
1	1	0	Memory read
1	1	1	Memory write